SPECIAL SPECIFICATION

6861

ATM Communication Backbone Switch

1. **Description.** This Item will govern the furnishing and installation of the ATM communications backbone switch at designated communications hubs/satellites as shown on the plans and as detailed in accordance with this Special Specification. All switches will be of the same manufacturer.

There will be three types of communication switches. Switches Type 1 and Type 2 will be sized to operate at a SONET OC-12 optical rate, with a non-blocking switch capacity of 10 Gbps, minimum. Switch Type 3 will be sized to operate at a SONET OC-3 optical rate, with a non-blocking switch capacity of 2.5 Gbps, minimum, as shown on the plans.

2. **Materials.**

   (1) **General Requirements.** All materials furnished, assembled, fabricated or installed under this Item will be supported by ATM Forum, IETF, and ITU (CCITT) standards, and be compliant with USER Network Interface (UNI) v3.0 specification for signaling-based, addressing, traffic management, and network management, while also supporting classical IP and LAN emulation.

   (2) **Functional Requirements.** The ATM switches will provide the transport and routing of all data, video, and voice communications for the Traffic Management System.

   The architecture of the switches will be composed of three major subsections: A switch fabrics, one or more network modules, and an integrated switch control processors. The switch fabric will be a non-blocking, 64-bit, contentionless, time division multiplexed (TDM) bus, running at 40 MHz, minimum, providing 2.5 Gbps of bandwidth. The switch control processors will be running at 400 MHz minimum.

   The switches will be single stage switches. The switch fabric will perform the VPI/VCI translation and bandwidth policing for the ATM cells received from the network modules. The switch fabric will also add a route word to each cell to indicate the appropriate destinations, and send the cells to the output queue circuitry.

   The switch will be designed around a non-blocking distributed shared memory, call switching bus. There will be four unidirectional 2.5 Gbps transmit busses, one for each switching fabric. The inputs from the various network modules on the fabrics will be time division multiplexed onto 64 bit sections of 256 bit space division backplane. The output section of each switch fabric will read from all of the input bus lines simultaneously, up to a maximum of 10 Gbps.

   The following interfaces will be available: DS1/T1, DS3/T3, OC-3c/STM-1, and OC-12c/STM-4, 100 Mbps TAXI, 155 Mbps UTP, OC 48c/STM 16, and Gigabit Ethernet.
End to end bandwidth management will be provided with the network, including capabilities such as Per-VC Queuing, Smart Buffers, Early Packet Discard (EPD), and Partial Packet Discard (PPD).

An integral switch control processor will used to configure and manage the switch, and to route connections.

The ATM switch will provide non-blocking TDM switching. The switching fabric will allow all input and output ports to transmit at their maximum rate with no chance of blocking or congestion within the switching fabric. The sum of all the ports time slots on the network modules will not exceed the total capacity of the switch. The switching fabric will support up to four OC-12c/STM-4 (622 Mbps) UNI Interfaces, and be compatible with one OC-48c/STM-16 (2.5 Gbps) without hardware modification.

The contentionless time division architecture will have a delay associated with cell transit of less than 15 microseconds, with a nominal latency delay of 10 microseconds.

The ATM switch will provide multicasting capabilities. As a cell traverses the switch fabric, each appropriate output port, part of the multicast, will read the cell information. Only a single cell will be transported through the switch fabric, regardless of how many ports are members of the multicast.

The switching fabric will support multiple ATM input/output speeds within a single ATM switching fabric. Since the traffic entering a port can use a variable number of time slots, higher speeds such as 2.5 Gbps will be supported.

All switching fabric network modules will be hot-swappable, including power supplies, CPUs, and switch fabrics. All switches will be fault-tolerant, maintaining an image of the network's configuration and utilization within each individual switch, so the loss of a switch is detected by the rest, and appropriate adjustments and rerouting are made automatically. Traffic will be load-balanced across the network, with all switches auto-configured by the other switches upon entry to the network.

The ATM switches will have only one switching stage, providing the lowest possible ATM switch latency.

The ATM switches will have an output buffer capacity of 13,312 cells with the ability to automatically and dynamically allocate space based upon a connection's service level requirements.

The switch will distinguish amongst virtual circuits and allocate each virtual circuit its own output buffer. Each connection will be treated independently, serviced in turn according to its requirements. Per-VC queuing will be provided to guarantee multiple levels of service and perform packet level discard, providing a dedicated queue for each virtual circuit, with each network module supporting up to 12,000 virtual circuits.

Each port will have three service levels for cell delay variation: Low (CDV), medium (CDV), or unspecified CDV. These cell delay variation specifications correlate to the requirements for constant bit rate (CBR) traffic, variable bit rate (VBR) traffic, and available/unspecified bit rate (ABR/UBR) traffic, respectively.
Each of these service levels will have 127 sublevels to provide fair access to the
network, supplying a total of 381 service priorities. The switch will automatically set
the service priority according to the connection’s requirements.

The ATM switch will include two complementary packet level discard techniques:
Partial Packet Discard (PPD), and Early Packet Discard (EPD).

Each network module will use output buffers to establish the non-blocking TDM
design, eliminating the need for input and intra-fabric buffers, by ensuring that each
input port has a time slot.

The type 3 ATM switch will be configurable from two to 24 ports per switch,
supporting up to 4 LAN/WAN network modules in any LAN/WAN combination. The
type 1 and 2 ATM switches will be configurable from two to 96 ports per switch,
supporting up to 16 LAN/WAN network modules in any LAN/WAN combination.
Both types of switches will be modular allowing the switches to grow. The following
network interfaces will be available:

- 622 Mbps OC-12c/STM-4, (1 port), Single Mode Intermediate Reach Fiber
- 622 Mbps OC-12c/STM-4, (1 port), Multi-Mode Fiber
- 155 Mbps OC-3c/STM-1, (4 port), Single Mode Short Reach Fiber
- 155 Mbps OC-3c/STM-1, (4 port), Single Mode Long Reach Fiber
- 155 Mbps OC-3c/STM-1, (4 port), Multi-Mode Fiber
  - 155 Mbps OC-3c/STM-1, (3 port), Multi-Mode Fiber, (1 port), Short Reach
    Single Mode Fiber
  - 155 Mbps OC-3c/STM-1, (3 port), Multi-Mode Fiber, (1 port), Long Reach
    Single Mode Fiber
- 155 Mbps OC-3c/STM-1, (4 port), UTP Category 5 Copper
- 100 Mbps TAXI (6 port), Multi-Mode Fiber
- 45 Mbps DS-3 (2 port)
- 45 Mbps DS-3 (4 port)
- 1.5 Mbps DS-1 (T1) (2 port)
- 1.5 Mbps DS-1 (T1) (6 port)
- 2.5 Gbps OC 48c/STM 16, (1 port), Single Mode Long Reach
- Gigabit Ethernet (1 port)
The ATM switches will be capable of operating from an input voltage of -48 volts DC with an input voltage tolerance of -36 volts to -76 volts DC, and also an input voltage of 120/240 volts AC at 2.3/1.3 amps maximum, supported with an input voltage tolerance of 97 volts to 260 volts AC, at 47 Hz to 63 Hz.

The ATM switch will have dual-redundant, load sharing, hot-swappable power supplies. Each ATM switch will be UL 1950 approved.

Each ATM switch will be capable of operating within a temperature range of 14º to 122ºF, with a relative humidity up to 95 percent, non-condensing.

3. **Construction.**

   (1) **General.** The equipment design and construction will utilize the latest available techniques with a minimum number of parts, subassemblies, circuits, cards and modules to maximize standardization and commonality.

   The equipment will be designed for ease of maintenance. All components will be readily accessible for inspection and maintenance.

   (2) **Electronic Components.** All electronic components will comply with Special Specification, "Electronic Components."

4. **Documentation Requirements.** The documentation requirements will be in accordance with Special Specification, "Testing, Training, Documentation, Final Acceptance and Warranty."

5. **Testing.** The testing will be in accordance with Special Specification, "Testing, Training, Documentation, Final Acceptance and Warranty."

6. **Training.** The training will be in accordance with Special Specification, "Testing, Training, Documentation, Final Acceptance and Warranty."

7. **Warranty.** The warranty will be in accordance with Special Specification, "Testing, Training, Documentation, Final Acceptance and Warranty."

8. **Measurement.** This Item will be measured as each unit furnished, installed, made fully operational, and tested, in accordance with these special specifications, or as directed.

9. **Payment.** The work performed and materials furnished in accordance with this Item and measured as provided under "Measurement" will be paid for at the unit price bid for "ATM Communications Switch" of the types specified. This price will be full compensation for furnishing all equipment described under this item, with all cables and connectors, and for furnishing all labor, materials, training, equipment, and incidentals.